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Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0027C	Serial No. 10/814,868	
Information Disclosure Statement by Applicant	Applicant: Christopher J. Diorio		
(Use several sheets if necessary)	Filed: March 30, 2004	Group: 2827	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
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SM	B	4,541,073	9/10/1985	Brice et al.			
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Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

SM	R	Declercq et al., "Design and Optimization of High-Voltage CMOS Devices Compatible With a Standard 5 V CMOS Technology", IEEE Custom Integrated Circuits Conference, 1993, pp. 24.6.1-24.6.4.
SM	S	Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique", IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 3, June 1976, pp. 374-378.
SM	T	Invitation to Pay Additional Fees for PCT/US 03/31792 date of mailing April 2, 2004.

Examiner /Son Mai/ (04/26/2006)	Date Considered 04/26/2006

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.